Guidelines to work on Test & power projects

* Check the given RT level design with a testbench for any design on either Model-Sim or VCS to get the correct output.
* Synopsys Design Compiler (DC) is used for synthesis, report generation , as an ATPG and for power analysis – to start DC use the command “design\_vision”, for tetramax use “tmax”.
* In synthesizing a design in Synopsys design compiler, there are 4 basic steps:
  + Analyze & Elaborate
  + Apply Constraints
  + Optimization & Compilation
  + Inspection of Results

**1) Analyze & Elaborate**

The analyze command will do syntax checking and create intermediate files which will be stored in the directory work, the defined design library.

The elaborate command goes to the work directory to pick up the files and builds the design up to the Design Compiler memory.

**2) Apply Constraints**

The **link command**checks to make sure all parts in the current design are available in Design Analyzer's memory.

The command **uniquify**is used to make unique the instances of the same reference design during synthesis.

The clock constraints are set up next followed by the input and output pins.

**3) Optimization & Compilation**

Maximum area is set to ‘0’.

The design is checked and compiled(the effort is set to medium)

Now the schematic can be viewed, and on that the critical delay path can be viewed by delay\_type to max.

**4) Inspection of results**

The 4 reports are taken which are they are timing, area, cell and power. The. syn

file is then generated and is saved into the src folder which contains all the library

files.

* Use the given tutorials to formulate .tcl files so you can source them in DC.
* To make the design testable scan cells need to be replaced in place of regular flops using the given manual to check how this can be accomplished.
* Using Tetramax requires all the individual gates as a library then your scan enabled design and a .spf file to be added to check for DRC and this flow is better explained in the given manual and tutorials as well.
* All submission in each phases should include have separate .tcl relevant figures and reports wherever necessary.